CONTINUATION/DIVISIONAL APPLICATION TRANSMITTAL

(Rule 53(b) Continuation or Divisional) ☐ DUPLICATE

Address to: **Assistant Commissioner for Patents** **Box PATENT APPLICATION** **Washington, D.C. 20231**	Attorney Docket No.: JEK/Haghiri First Named Inventor: Yahya HAGHIRI-TEHRANI et al. Total Pages:

This requests a ☐ Continuation or ☒ Divisional application under 37 CFR 1.53(b) of prior application:

Appl. No.:	08/686,026	Group Art Unit:	2835
Filed on:	25 July 1996	Examiner:	J. Gandhi
Entitled:	CIRCUIT UNIT AND A METHOD FOR PRODUCING A CIRCUIT UNIT		

☐ 1. The entire disclosure of the pending, prior application is hereby incorporated by reference.

☒ 2. Submitted herewith is a copy of the complete prior application as filed.

☐ 3. This application is filed by fewer than all the inventors named in the prior nonprovisional application, 37 CFR 1.53(b)(1). **DELETE** the following inventor(s): _____.

☒ 4. Submitted herewith is a copy of the signed Oath/Declaration from the prior application.

☐ 5. Small entity status was established in the prior application, and is still proper and desired.

☐ 6. A _____ month Petition for Extension of Time is filed concurrently in the prior application.

☒ 7. The Commissioner is authorized to credit any overpayment and charge any deficiency in any fees required under 37 CFR 1.16 and/or 1.17 to Deposit Account No. 02-0200.

☒ 8. A check in the amount of $ 760.00 is submitted herewith.

☒ 9. Insert before the first sentence of the specification: -- This application is a ☐ Continuation ☒ Division of nonprovisional application serial number 08/686,026 filed 25 July 1996 . --

☐ 10. Cancel in this application original claims _____ of the prior application before calculating the filing fee. At least one independent claim is retained.

☒ 11. The prior application is assigned of record to: Giesecke & Devrient GmbH.

☒ 12. Priority is claimed based on each foreign application so listed in the Oath/Declaration and a certified copy of each was filed in U.S. application number 195 27 359.1 filed 26 July 1995.

☒ 13. A Preliminary Amendment is enclosed.

☐ 14. Other: _____.

THE FILING FEE IS CALCULATED AS FOLLOWS:				Basic Fee:	$760.00
Total Claims:	11	- 20 =		X $18 =	
Independent Claims:	3	- 3 =		X $78 =	
Correspondence Address: BACON & THOMAS, PLLC, 625 Slaters Lane, 4th Floor, Alexandria, VA 22314-1176				Multiple Dependent Claim (add $260 00):	
				Subtotal:	760 00
				50% Reduction if Small Entity Status:	
Phone: 703-683-0500 Fax: 703-683-1080				Total:	760.00

Date:	Name.	Signature:	Reg. No.
09 December 1999	J. ERNEST KENNEY		19,179

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(16Nov1998)

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	)	
	)	
Yahya HAGHIRI-TEHRANI et al.	)	**Group Art Unit: unassigned**
	)	
Serial Number: Not yet assigned	)	**Examiner: unassigned**
	)	
Filed: 03 December 1999	)	
	)	

For: METHOD FOR PRODUCING A CIRCUIT UNIT

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Prior to calculation of the filing fees and examination on the merits, please amend this application as follows:

IN THE DRAWINGS:

Please amend Figures 2, 3, 7 and 9 as marked in red on copies of the drawings appended hereto.

In Figure 2, the cross-section has been identified at III-III instead A-A.

In Figure 3, elements are provided with reference numerals.

In Figure 7, the material filling the through holes is properly identified as 13a and the through holes are properly identified as 13.

In Figure 9, the material extending through the through hole is identified as 13.

THE EXAMINER'S APPROVAL OF THE PROPOSED DRAWING AMENDMENTS IS RESPECTFULLY REQUESTED.

Divisional Application of
Yahya HAGHIRI-TEHRANI
Filed: 09 December 1999

IN THE SPECIFICATION:

Page 1, please change the title of the invention to --METHOD FOR PRODUCING A CIRCUIT UNIT--;

Page 1, before the first line of text, insert the centered headings:

--BACKGROUND OF THE INVENTION

1. FIELD OF THE INVENTION--;

before the first and second paragraphs, insert the centered heading:

--RELATED TECHNOLOGY--.

Page 2, between lines 9 and 10, insert the following:

--From US 4,960893 (Inoue) a circuit unit in the form of an IC card is known. The IC card comprises an electronic module with a coil structure being formed on the semiconductor substrate of the electronic module. A coil may be formed of two or more coil structures which are deposited on different metallic layers having insulation layers between the metallic layers whereat the metallic layers are interconnected by means of a central conductive member which extends between the distinct metallic layers.

However, the Inoue patent teaches forming the coil on the substrate of the IC chip. As the production of semiconductor devices is very expensive and the yield depends directly on the area of semiconductor covered by the IC chip, the teaching of Inoue has both the disadvantage of high cost and low yield as the area covered by the an IC comprising coil structure is enormous. The size of the IC chip has the further disadvantage of being susceptible to mechanical stress. The IC chip is embedded in the card body which is flexible therefore torsion or bend may destroy the IC card or the IC chip.

From JP 6 336096 a chip card is known which is produced from two insulating substrates. Each of the substrates has a coil pattern. After connecting the two substrates by an insulating adhesive the two coil patterns form one coil.

However, as it is stated expressly not to use a through hole for contacting the two coil patterns and as the coil patterns are formed on different substrates, chip cards having coil layers and insulating layers which are applied alternately to a substrate are discouraged.

From EP 0 547 563 B1 a printed circuit board antenna is known which has a plurality of different coil layers. However the European patent does not show the use of an IC chip. In particular this is a disadvantage because the two coil ends are on different sides of the circuit board. If an IC chip is to be mounted on one side of the circuit board an additional through hole is necessary to connect the IC to the second end of the coil. Additional connectors are also necessary to connect the different layers of the coil which is especially a disadvantage because an additional step is necessary to insert the connectors.--;

line 15, delete this line entirely and substitute therefor the centered heading:

--BRIEF SUMMARY OF THE INVENTION--.

Page 2, last paragraph, line 3, change number "44 16 197.4" to --44 16 697.4--;

Page 3, between the third and fourth paragraphs, insert the centered heading:

--BRIEF DESCRIPTION OF THE DRAWINGS--;

line 27, change "A-A" to --III-III--.

Page 4, before the first line, insert the centered heading:

--DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS OF THE INVENTION--

;

line 7, before "ends" insert --free--;

line 19, after "layer" insert --section--;

line 20, after "layer" insert --section--;

line 21, after "layer" insert --section--;

line 27, after "layer" insert --section--;

line 29, after "layer" insert --section--;

line 30, after "layer" insert --section--;

line 31, before "end" insert --first--; after "layer" insert --section--;

line 32, change "end" to --second end area--; after "layer" insert --section--

Page 5, line 1, after "layer" insert --section--;

line 3, after "layer" (both occurrences) insert --section--;

line 4, after "layer" insert --section--;

line 6, change "layers" to --layer sections--;

line 8, change "layers" to --layer sections--;

line 14, change "layers" to --layer sections--;

line 16, change "layers" to --layer sections--;

line 17, after "that" insert --first--; after "layer" insert --section--; after "on" insert --(e.g. layer 9)--;

line 19, after "layer" insert --section (e.g. layer 17)--;

line 20, after "overprint" insert --first--; after "layer" insert --section--;

line 22, after "printed" insert --first--; before "which" insert --of the coil layer sections--;

line 24, before "end" insert --first--; after "layer" (each occurrence) insert --section--;

line 26, after "from" insert --first--;

line 28, change "layers" to --layer sections--;

line 30, after "coil" insert --section--;

line 32, after "layer" insert --section--;

line 33, change "end" to --first ends--; change "layer" to --layers--.

Page 6, line 1, after "layer" insert --section--;

line 2, after "internal" insert --or second--;

line 3, after "layer" (first occurrence) insert --section--; after "with" insert --second end of--; after "9" insert --(Figure 3)--; after "external" insert --first--;

line 6, after "layer" insert --section--; after "free" insert --first--;

line 8, after "layer" insert --section--;

line 10, after "covering" insert --insulating--;

line 14, after "with" insert --first--; after "coil" insert --formed by electrically connected sections 9 and 17--;

line 22, change "A-A" to --III-III--;

line 23, after "layer" insert --section--;

line 25, after "layer" insert --section--;

line 26, after "layer" insert --section--; after the sentence ending with the numeral "9", insert the following:

--Layer 17 is located farther from the substrate 1 than layer 9. Second ends 15a and 19a of layers 9 and 17 overlap at the window 13 in insulating layer 11. A portion 11a of layer 11 overlaps second end 15a of layer 9.--

Page 7, line 1, change "Fig. 4 shows" to --Figs. 4A and 4B show--;

line 2, after "coil" insert --first--;

line 31, change "Fig. 5 shows" to --Figs. 5A and 5B show--.

Page 8, line 27, after "layer" insert --section--;

line 28, after "layer" insert --section--;

line 31, change "layers" to --layer sections--;

line 32, change "compound" to --composite--;

line 34, after "layer" (each occurrence) insert --section--;

line 35, change "layers" to --layer sections--.

Page 9, line 2, change "layers" to --layer sections--;

line 5, change "layers" (each occurrence) to --layer sections--;

line 8, change "layers" to --sections--;

line 12, before "coil" insert --ends of--; change "layers" to --sections--;

line 14, change "Fig. 8 coil layers" to --Fig. 7 ends of coil sections--;

line 17, before "coil" insert --the end of--; after "layer" insert --section--;

line 18, before "coil" insert --the end of--; after "layer" insert --section--;

line 19, change "layers" to --sections--;

line 20, after "layer" insert --section--;

line 22, change "layers" to --layer sections--;

line 25, change "layers to --layer sections--;

line 28, before "coil" insert --ends of--; change "layers" to --layer sections--;

line 30, change "layers" to --layer sections--;

line 31, change "Fig. 10" to --Figs. 10A and 10B--;

line 32, before "coil" insert --ends of--; change "layers" to --layer sections--;

line 35, after "layer"insert --section--.

Page 10, line 1, after "layer" insert --section--;

line 2, after "layer" (each occurrence) insert --section--;

line 4, after "layer" insert --section--;

line 12, after "layer" insert --section--;

line 14, after "layer" insert --section--;

line 16, after "layer" insert --section--;

line 20, change "layers" to --layer sections--;

line 21, change "layers" to --sections--.

IN THE ABSTRACT:

Change line 1 to read: --A circuit unit having a--.

Line 4, change "layers" to --layer sections--.

Line 5, change "layers" to --layer sections--.

Line 7, before "coil" insert --first--.

Divisional Application of
Yahya HAGHIRI-TEHRANI
Filed: 09 December 1999

IN THE CLAIMS:

Please cancel claims 1 -11 and 23, without prejudice or disclaimer.

Please amend claims 12-22 as shown on the appended APPENDIX OF CLAIMS.

REMARKS

Examination of the application as amended is respectfully requested.

Respectfully submitted,
BACON & THOMAS, PLLC

J. ERNEST KENNEY
Attorney for Applicants
Registration Number 19,179

BACON & THOMAS, PLLC
625 Slaters Lane, Fourth Floor
Alexandria, Virginia 22314

Telephone: (703) 683-0500
Facsimile: (703) 683-1080

Date: December 9, 1999

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A circuit unit and a method for producing a circuit unit

This invention relates to a circuit unit comprising at least an insulating substrate on which a conductive coil is located, and an integrated circuit whose connection points are electrically connected with the coil ends. The invention relates further to a method for producing such a circuit unit.

Circuit units of the above type are known from the prior art, being designed for example as compact electronic modules which are inserted in chip cards for noncontacting data exchange with a terminal. For example US-PS 4,999,742 discloses a circuit unit in the form of an electronic module with an insulating substrate on which a ring-shaped wound coil is glued. The coil ends are guided into the receiving space arising through the ring-shaped coil, and electrically connected there with the connection points of an integrated circuit. The receiving space for the integrated circuit and coil ends is cast with a casting compound for protecting these sensitive components from mechanical loads.

The electronic module known from US-PS 4,999,742 has a compact structure but the coil must be wound in a separate method step and glued on the insulating substrate in a further method step.

However, the as yet unpublished German patent application P 44 16 697.4 discloses a circuit unit in the form of a chip card having printed on one card layer of the multilayer card body a coil from a conductive lacquer whose ends are electrically connected with the connection points of an integrated circuit.

The structure of the circuit unit known from patent application 44 16 697.4 has the advantage that the coil is printed directly on a card layer so that the method step of applying a separately manufactured coil to an insulating sub-

strate is omitted. For some applications of the circuit unit, however, it is desirable for the coil to have a higher number of turns than can be realized with the structure explained above. Furthermore it may be desirable to provide the circuit unit with relief embossing. One must then make sure the printed turns of the coil, which are generally formed as a very thin layer, are not interrupted. Also, the production method for the circuit unit should be further optimized with regard to inexpensive mass production.

It is therefore the problem of the invention to further improve the abovementioned circuit unit and at the same time in particular to extend its range of applications. It is further the problem of the invention to propose a method for producing such a circuit unit.

This problem is solved by the independent claims.

One advantage of the invention is to be seen in that a higher number of turns can be realized than on the structure known from German patent application 44 16 197.4. The coil can still be applied directly to the substrate of the circuit unit so that an additional method step for applying a separately manufactured coil is unnecessary. This is made possible by the fact that coil layers and insulating layers are applied alternately to the insulating substrate, the individual coil layers being electrically interconnected via plated-through holes so as to yield a coil. The coil layers and insulating layers are preferably printed on. Alternatively it is also possible for the insulating layers to consist of thin insulating foils on which the coil layers are printed on one or both sides. The throughplating through the insulating layers can be done in the simplest case by providing windows or holes in the insulating layers through which the conductive material of the coil layers penetrates when the coil layers are printed on or the layers laminated together. Additional conductive material can likewise be applied for throughplating, or additional conductive elements provided.

A further advantage of the invention is to be seen in that the circuit unit can be manufactured especially easily by the multiple-copy method, since one can apply the coil layers and also the insulating layers (depending on the embodiment) using printing technology, with which multiple-copy production is commonplace.

Furthermore the invention has the advantage that the coil ends can be adapted especially easily to the various possibilities of forming the electric connection between the coil ends and the connection points of the integrated circuit.

Furthermore it is advantageous that the invention permits relief embossing of the circuit unit without restriction, with no danger of one or more turns of the coil being interrupted. For this purpose the turns of the coil are guided outside the relief embossing area of the circuit unit or between the individual relief embossing lines, whereby the width of the turns can be greater than the line spacing for compensating production tolerances, or the turns run in the area of the embossed characters but are wider than the character size.

Some embodiments and further advantages of the invention will be explained in connection with the following figures, in which:

Fig. 1 shows a circuit unit in a plan view,

Fig. 2 shows a circuit unit in a perspective view,

Fig. 3 shows a cross section along line A - A of Fig. 2,

Figs. 4, 5 show embodiments for contacting a coil with an integrated circuit or module,

Figs. 6 to 10 show embodiments for throughplating for forming an electric connection between opposite coil layers in cross section,

Fig. 11 shows a circuit unit with marked relief embossing fields in a plan view,

Figs. 12, 13 show embodiments for forming and arranging turns of a coil as an enlarged detail in a plan view.

Fig. 1 shows systematically a circuit unit in the form of a chip card for noncontacting data exchange in a plan view. The dimensions of such chip cards are identical with the dimensions of chip cards for contacting data exchange, which are fixed in ISO standard 7810. The circuit unit contains insulating substrate 1 in the form of a card layer on which coil 3 is located whose ends 15 and 19 are electrically connected with the connection points of integrated circuit 7. The integrated circuit can also be cast into a module which, for easier contacting of integrated circuit 7, has contact surfaces which are electrically connected with the connection points of integrated circuit 7. The turns of coil 3 run along the outer edge of the card layer, yielding a large-area coil in the interests of high energy input.

Fig. 2 shows a perspective view not true to scale of an inventive circuit unit which is produced as described in the following. On insulating substrate 1, which exists e.g. in the form of a card layer (see Fig. 1) one first applies first coil layer 9, which is dash-lined in Fig. 2 and can contain a plurality of turns (coil layer 9 shown contains only one turn in order not to complicate the drawing). Coil layer 9 is preferably printed on with a conductive lacquer, but it is also possible to spray on the coil layer using a corresponding mask, or to etch it out of a conductive coating located on the substrate. Other production techniques are conceivable.

After applying coil layer 9 one applies to insulating substrate 1 insulating layer 11, which is hatched in Fig. 2 and covers the turns of coil layer 9. Insulating layer 11 has window 13 and is applied to coil layer 9 in such a way that end 15 of coil layer 9 is not covered thereby and at least the end of the last turn of coil layer 9 is accessible through window 13. Insulating layer 11 is preferably likewise printed on, but it is also possible here to spray it on using a corresponding mask or to use as insulating layer 11 a thin insulating foil, etc.

In a further method step one applies further coil layer 17 to insulating layer 11 using the same techniques as for applying coil layer 9. Further coil layer 17 is preferably also printed on. Coil layer 17 is electrically connected with coil layer 9 through window 13 in insulating layer 11, yielding coil 3 consisting of coil layers 9 and 17. One can facilitate the formation of an electric connection between coil layers 9 and 17 by making the coil ends which are electrically interconnected wider than the turns of the coil, as also shown in Fig. 2. It is easy to realize such widening by printing technology. Details on the connecting technique will be described below.

One can optionally repeat the application of further insulating layers and coil layers in the explained manner once or several times until circuit unit coil 3 composed of the coil layers has the desired number of turns. One must thereby make sure that end 15 of the coil layer first printed on is not covered, and that the circuit unit does not exceed a predetermined height. When printing on the last coil layer one can overprint end 15 of the first printed coil layer with a conductive lacquer again. One then obtains two freshly printed coil ends 15 and 19 which can be electrically connected with the integrated circuit especially easily.

End 19 of the last applied coil layer, i.e. coil layer 17 in Fig. 2, is applied in such a way that it is especially easy to form an electric connection from coil ends 15 and 19 to integrated circuit 7. In the embodiment of the invention shown in Fig. 2 the coil layers and insulating layers are applied to insulating substrate 1 in a kind of frame. In the shown embodiment, coil ends 15 and 19 are guided into the interior of the frame onto insulating substrate 1. One avoids superimposition of turns in a coil layer by guiding the internal end of the particular coil layer into the part enclosed by the frame, as shown in Fig. 2.

By suitable choice of the coil ends which are electrically connected with the integrated circuit one can always

avoid superimposition of turns in a coil layer. For example, if coil end 19 is to be outside the frame the internal end of coil layer 17 is connected with coil layer 9 and the external end of coil layer 17 guided outward.

Alternatively it is also possible to apply an insulating layer with a window to the last coil layer, whose free end is connected with the integrated circuit. Through the window the free coil end can then be guided over the coil layer in any direction, since no short-circuit can occur between the turns of the coil because of the covering layer.

According to the embodiment of Fig. 2 one applies integrated circuit 7 to the noncovered part of insulating substrate 1, electrically connecting the connection points of the circuit with ends 15 and 19 of the resulting coil e.g. by means of bonding wires 21. One can simplify the formation of the electric connections from integrated circuit 7 to coil ends 15 and 19 by making the coil ends wider than the individual turns of the coil. For this purpose one need only accordingly adapt the artwork or, if the coil layers sprayed on, the masks used. No separate method steps are thus necessary for producing widened coil ends.

Fig. 3 shows a cross section along line A - A of Fig. 2 to illustrate the sequence of layers. Coil layer 9 is applied to insulating substrate 1, being covered by insulating layer 11 containing window 13 through which further coil layer 17 is electrically connected with coil layer 9. Further insulating layers and coil layers can follow alternately.

In a variant the connection between integrated circuit 7 and coil ends 15 and 19 is not formed via bonding wires but by directly mounting integrated circuit 7 on coil ends 15 and 19. For this purpose integrated circuit 7, or module 23 containing integrated circuit 7, can either be mounted on coil ends 15 and 19 already applied, or circuit 7 or module 23 is first inserted in substrate 1 and then overprinted with coil ends 15 and 19.

Fig. 4 shows cross sections of two embodiments of the inventive circuit unit wherein coil ends 15 and 19 were first printed on substrate 1, and module 23 or integrated circuit 7 then mounted on coil ends 15 and 19. Module 23 or integrated circuit 7 can be mounted either directly after the printing operation or only after a short period of time in which the printed conductive lacquer dries at least partly.

Fig. 4a shows substrate 1 with printed coil ends 15 and 19 and module 23. Module 23 contains integrated circuit 7 which is coated by casting compound 8 and whose connection points 27 are electrically connected with contacts 25 of module 23 via bonding wires. Module 23 is mounted on coil ends 15 and 19 in such a way that contacts 25 of module 23 touch coil ends 15, 19. The arrangement shown in Fig. 4a can be covered by a cover foil not shown in the figures, which optionally contains a gap for module 23. In the embodiment shown in Fig. 4a, module 23 is mounted on coil ends 15 and 19 in such a way that casting compound 8 points away from coil ends 15 and 19. However it is also possible to mount the module turned by 180°. In this case one should provide a corresponding gap in substrate 1 for partly receiving casting compound 8. This variant is used in particular when a low overall height of the circuit unit is to be achieved.

Fig. 4b again shows substrate 1 with printed coil ends 15 and 19. Integrated circuit 7 is mounted on coil ends 15 and 19 in such a way that connection points 27 of integrated circuit 7 touch coil ends 15, 19. As in the embodiment of Fig. 4a, the structure shown in Fig. 4b can also be protected by a cover foil not shown, which can optionally contain a gap for integrated circuit 7.

Fig. 5 shows cross sections of two embodiments of the inventive circuit unit whereby module 23 or integrated circuit 7 is overprinted for contacting with coil ends 15 and 19.

In Fig. 5a module 23 is fit into substrate 1 in such a way that the surface of module 23 is flush with the surface

of substrate 1. Coil ends 15 and 19 printed on after insertion of module 23 in substrate 1 extend over the surface of module 23 so far that they partly cover contacts 25 of module 23 so as to form an electric connection between contacts 25 and coil ends 15 and 19.

In Fig. 5b integrated circuit 7, instead of module 23, is inserted into substrate 1 in such a way that the surface of integrated circuit 7 is flush with the surface of substrate 1 and connection points 27 of integrated circuit 7 point upward. Coil ends 15 and 19 are printed on substrate 1 in such a way that they extend over connection points 27 of integrated circuit 7. This forms an electric connection between connection points 27 and each coil end 15 and 19. For embedding integrated circuit 7 in substrate 1 one can either provide a corresponding gap, or press the chip into substrate 1 using heat and pressure.

Some variants for throughplating will now be described with which one can form electric connections between two coil layers or between a coil layer and connection point 27 of integrated circuit 7 or contact 25 of module 23 through insulating layer 11, for example a thin insulating foil.

Fig. 6 shows an embodiment of the inventive circuit unit in cross section, in which the throughplating takes place when the individual layers of the circuit unit are laminated together. One can see the sequence of layers of the circuit unit before the laminating process.

According to Fig. 6 substrate 1a with coil layer 17 and substrate 1b with coil layer 9 are separated from each other by insulating foil 11. Window 13 is provided in foil 11 by punching, piercing or by laser beam at a place where coil layers 9 and 17 are opposite each other. Lamination produces a compound from individual layers 1a, 1b and 11. Simultaneously the laminating process forms an electric connection between coil layer 9 and coil layer 17 through window 13. This can be supported by applying to at least one of coil layers 9 and 17 opposite window 13 a small portion of conductive adhe-

sive 29 which flows into window 13 during lamination, thereby forming an electric connection between coil layers 9 and 17.

Fig. 7 shows an embodiment of the inventive circuit unit in cross section, in which insulating foil 11 is printed with coil layers 9, 17 one on each side, with layers 9 and 17 partly overlapping. In the overlap area insulating foil 11 has one or more windows 13 which are produced for example by punching, piercing or by laser beam. When coil layers 9 and 17 are printed on insulating foil 11 by the screen printing method, windows 13 are filled with the printing material, for example a conductive lacquer, thereby forming electric connections between coil layers 9 and 17.

Fig. 8 shows a further embodiment for throughplating. As in Fig. 8 coil layers 9 and 17 are applied to the opposite sides of insulating foil 11 so that they partly overlap. In the overlap area at least one thin wire 31 is slipped in to penetrate coil layer 17, insulating foil 11 and at least partly also coil layer 9, thereby forming an electric connection between coil layers 9 and 17. Wire 31 can also be fed completely through coil layer 9 and bent at its end by a suitable apparatus. To facilitate the feedthrough of wire 31 one can heat it in one variant of the embodiment.

Fig. 9 shows an embodiment in which coil layers 9 and 17 are first applied to the opposite sides of insulating foil 11. At least one window 13 is then provided in coil layers 9 and 17 and intermediate insulating foil 11, for example by punching, piercing or by laser beam, in the area where opposite coil layers 9 and 17 overlap. Window 13 is finally filled with conductive adhesive 33 and an electric connection thus formed between coil layers 9 and 17.

Fig. 10 shows an embodiment in which an electric connection can be formed between coil layers 9 and 17 by means of connecting element 35.

Fig. 10a shows the sequence of layers of the circuit unit before the laminating process. Coil layer 9 is applied to substrate 1. Above substrate 1 there is insulating foil 11

which carries coil layer 17 and has window 13 in an area opposite coil layer 9 and adjacent coil layer 17. Connecting element 35 is disposed on auxiliary carrier foil 37 above window 13 and overlapping with coil layer 17. Connecting element 35 can consist for example of a thermally activable conductive adhesive.

Fig. 10b shows the layer structure from Fig. 10a after lamination. The layers shown in Fig. 10a can be joined into a compound under pressure and heat by means of a conventional laminating press. The laminating press die pressing against the top of the structure is formed so that connecting element 35 is pressed through window 13 against coil layer 9 and connects therewith during the laminating process. The other end of connecting element 35 is pressed against coil layer 17 and connects therewith. This forms an electric connection between coil layers 9 and 17. Auxiliary carrier foil 37 comes off connecting element 35 during lamination and is then removed.

In a variant of the invention one can omit window or windows 13 in insulating layer 11. In this variant there is no electric connection between the individual coil layers. The coil layers are instead coupled capacitively. Capacitive coupling can also be used for coupling integrated circuit 7 with coil 3 so that an electric connection can likewise be omitted here.

A further aspect of the invention is that it eliminates restrictions that existed up to now with respect to relief-embossing a circuit unit containing coil 3. This can be done by various measures each applicable with both single-layer and multilayer coils 3.

Fig. 11 shows a circuit unit in a plan view, with dotted lines delimiting areas 37 and 38 within which relief embossing is admissible in chip cards according to ISO standard 7811. Relief embossing can be used for example to bring out letters and numbers or other characters. The embossed characters can be printed on a paper voucher with a suitable apparatus if required. However, embossing can damage coil 3.

Lower area 37 is especially problematic in terms of possible damage to turns of the coil, since coil 3 is generally required to have a large area and the turns therefore run close to the edge of the circuit unit.

Fig. 12 shows an enlarged detail of the circuit unit shown in Fig. 11 in a plan view. To prevent interruption of the turns of coil 3, turn 39 is disposed between relief embossing field 37 and the edge of substrate 1 in the embodiment according to Fig. 3. If there is enough room, several turns or even all turns of coil 3 can also run here. Since no embossing occurs in this area there is no danger of the turns of coil 3 being interrupted by the embossing process. With a multilayer coil the room becomes scarce at higher numbers of turns than with a single-layer coil, since not all turns have to be disposed side by side.

Turns 41 running in the area of relief embossing field 37 are so greatly widened that they are wider than the size of the characters embossed there. This ensures that turns 41 are not interrupted by the embossing process, even if the embossed characters would each sever a cross section of turns 41 corresponding to the character size. If there is not enough room for one or more turns 39 outside relief embossing field 37, all turns 41 can be guided through relief embossing field 37.

Fig. 13 likewise shows an enlarged detail of the circuit unit shown in Fig. 11 in a plan view. According to the embodiment shown in Fig. 13 the turns of coil 3 are guided either between relief embossing field 37 and the edge of the circuit unit (turn 39), or following the relief embossing lines or between the individual relief embossing lines (turns 43). Turns 43 running between the relief embossing lines or directly following the relief embossing lines are somewhat widened to compensate production tolerances. This ensures that at least a partial area of turns 43 runs on a surface which is not embossed so that there is no danger of turns 43 being interrupted. In the embodiment shown in Fig. 13 it also

depends on the exact dimension of the turns whether no turn at all, or at least one turn 39, can be guided past the relief embossing field, i.e. whether there is enough room for one or even for several turns 39 between relief embossing field 37 and the edge of the substrate. The turn variants shown in Figs. 12 and 13 can also be combined.

Besides the already outlined measures, others are also conceivable for preventing interruption of the turns of coil 3 by embossing. For example the properties of the coating material used for producing the turns can be adapted as greatly as possible to substrate 1 to which they are applied, so that the coating material does not crack and thus interrupt the turns during embossing. It is likewise conceivable to use as a coating material conductive plastics which are so elastic that they do not crack during embossing.

In the embodiments in which one or more turns 39 are guided between relief embossing field 37 and the edge of the circuit unit, the resistance of coil 3 might possibly assume inadmissibly high values since turns 39 must be very narrow due to the little room available. This problem can be counteracted by applying turns 39 in greater layer thicknesses, which can be done for example by multiple printing. It is likewise possible to reduce the resistance by widening turns 39 in the areas where enough room is available.

The circuit unit can be produced either in single piece production or via sheets or webs which are divided into individual circuit units at the end of production.

The described measures for improving the circuit unit, for example providing a multilayer coil structure whereby different throughplating variants are possible, permitting relief embossing of the circuit unit by suitably selecting the coil layer dimensions and pattern, optionally also material, and directly contacting the integrated circuit or module with the coil, can be used either singly or in combination.

Claims

1. A circuit unit comprising at least an insulating carrier substrate (1) on which a conductive, flat coil (3) is located, and an integrated circuit (7) whose connection points (27) are electrically connected with the coil ends (15, 19) directly or via contacts (25) or coupled capacitively therewith, **characterized** in that coil layers (9, 17) and insulating layers (11) are applied alternately to the insulating substrate (1), each insulating layer having at least one opening (13) through which the adjacent coil layers (9, 17) are electrically interconnected, or the adjacent coil layers (9, 17) being coupled capacitively, so that the individual coil layers (9, 17) yield a coil (3).

2. The circuit unit of claim 1, characterized in that the at least one opening (13) in the insulating layer (11) leads to one end of the coil layer (9) covered by the insulating layer (11), and this end of the coil layer (9) is electrically connected with one end of the coil layer (17) located on the insulating layer (11) through the at least one opening (13) in the insulating layer (11).

3. A circuit unit comprising at least an insulating carrier substrate (1) on which a conductive, flat coil (3) is located, and an integrated circuit (7) whose connection points (27) are electrically connected with the coil ends (15, 19) directly or via contacts (25), **characterized** in that the circuit unit has at least one relief embossing field (37) in the area of which characters are embossable on the circuit unit, and the dimensions and/or the arrangement of turns of the coil on the substrate (1) are selected so that the coil (3) is not completely severed during embossing of the characters.

4. The circuit unit of claim 3, characterized in that at least one turn (39) of the coil runs between the relief embossing field (37) and the edge of the substrate (1).

5. The circuit unit of any of claims 3 to 4, characterized in that the turns (41) of the coil are wider in the area of the relief embossing field (37) than the size of the embossed characters.

6. The circuit unit of any of claims 3 to 5, characterized in that the turns (43) of the coil run between successive lines of the relief embossing field (37).

7. The circuit unit of claim 6, characterized in that the turns (43) of the coil are wider in the area of the relief embossing field (37) than the distance between successive lines.

8. The circuit unit of claim 3, characterized in that the material properties of the coil (3) are adapted to the substrate (1) at least in the area of the relief embossing field (37) in such a way that no cracks inadmissibly impairing the function of the coil (3) arise in the coil material during embossing of the characters.

9. The circuit unit of claim 8, characterized in that the coil (3) consists of conductive plastic.

10. The circuit unit of any of claims 1 to 9, characterized in that the coil (3) is printed on the insulating substrate (1) or on the insulating layers (11).

11. A chip card, characterized in that it has the circuit unit of any of claims 1 to 10.

12. A method for producing a circuit unit comprising an insulating carrier substrate (1) on which a conductive coil (3) is located, and an integrated circuit (7) whose connection points (27) are electrically connected with the coil ends (15, 19) directly or via contacts (25), characterized by the following method steps:

a) applying a coil layer (9) with at least one turn to the substrate (1),

b) covering at least the area of the applied coil layer (9) with an insulating layer (11) containing at least one opening (13) through which at least one of the covered turns of the coil layer (9) is accessible,

c) applying to the insulating layer (11) a further coil layer (17) with at least one turn which is electrically connected with the previously covered coil layer (9) through the at least one opening (13),

d) optionally repeating method steps b) and c) once or several times,

e) electrically connecting the connection points (27) of the integrated circuit (7), or the contacts (25) of a module (23) containing the integrated circuit (7), with one end (15) of the coil layer (9) located directly on the insulating substrate (1), on the one hand, and with one end (19) of the last applied coil layer (17), on the other hand.

13. The method of claim 12, characterized in that the electric connection between the coil layers (9, 17) takes place through the at least one opening (13) in the insulating layer (11) by laminating the insulating layer (11) or insulating layers (11) and the insulating substrate (1).

14. The method of claim 13, characterized in that conductive material (29) is additionally disposed in the area of the at least one opening (13) before lamination.

15. The method of claim 12, characterized in that the at least one opening (13) in the insulating layer (11) is produced before application of at least one of the coil layers (9, 17) separated by the insulating layer (11), and the at least one opening (13) is filled with the coil material during application of at least one of the coil layers (9, 17).

16. The method of claim 12, characterized in that the at least one opening (13) is filled with conductive material (33) after application of the coil layers (9, 17) so as to form an electric connection between the coil layers (9, 17).

17. The method of claim 12, characterized in that a conductive element (35) is transferred to the coil layers (9, 17) in such a way that the conductive element (35) forms an electric connection between the coil layers (9, 17) through the at least one opening (13).

18. The method of claim 12, characterized in that the at least one opening (13) is produced by means of at least one wire (31) piercing the insulating layer (11) and at least partly the coil layers (9, 17) separated by the insulating layer (11), the wire (31) remaining in the insulating layer (11) and at least partly in the coil layers (9, 17) so as to form an electric connection between the coil layers (9, 17).

19. A method for producing a circuit unit comprising an insulating substrate (1) on which a conductive, flat coil (3) is located, and an integrated circuit (7) whose connection points (27) are electrically connected with the coil ends (15, 19) directly or via contacts (25), **characterized** by the steps of:

applying the coil (3) to the substrate (1) in such a way that the distance between the coil ends (15, 19) can be bridged by the connection points (27) of the integrated circuit (7) or by the contacts (25) of a module (23) containing the integrated circuit (7), and

mounting the integrated circuit (7) or the module (23) on the coil ends (15, 19) in such a way that the connection points (27) of the integrated circuit (7) and the coil ends (15, 19) or the contacts (25) of the module (23) and the coil ends (15, 19) touch, and

forming an electric contact between the connection points (27) and the coil ends (15, 19) or the contacts (25) and the coil ends (15, 19) solely through this touching.

20. The method of claim 19, characterized in that the coil (3) is printed on the substrate (1), and the integrated circuit (7) or the module (23) is mounted before the printing material completely dries.

21. A method for producing a circuit unit comprising an insulating carrier substrate (1) on which a conductive, flat coil (3) is located, and an integrated circuit (7) whose connection points (27) are electrically connected with the coil ends (15, 19) directly or via contacts (25), **characterized** by the steps of:

incorporating the integrated circuit (7) or a module (23) containing the integrated circuit (7) in the substrate (1) in such a way that the connection points (27) of the integrated circuit (3) or the contacts (25) of the module are flush with the surface of the substrate (1),

then applying the coil (3) to the substrate (1) in such a way that the coil ends (15, 19) at least partly cover the connection points (27) or the contacts (25), and

forming an electric contact between the connection points (27) and the coil ends (15, 19) or the contacts (25) and the coil ends (15, 19) solely through this direct touching.

22. The method of claim 21, characterized in that the coil (3) is printed on.

23. A chip card, **characterized** in that it has a circuit unit produced according to any of claims 12 to 22.

Abstract

The invention relates to a circuit unit comprising an insulating substrate (1) on which a conductive, flat coil (3) is located. The coil (3) can consist of a plurality of coil layers (9, 17) separated by insulating layers (11). To interconnect the individual coil layers (9, 17) into a coil, at least one opening (13) is provided in each of the insulating layers (11). The connection between the coil ends (15, 19) of the coil (3) and an integrated circuit (7) or a module (23) containing the integrated circuit (7) can be formed solely by the coil ends (15, 19) and the connection points (27) of the integrated circuit (7) or the contacts (25) of the module (23) touching. The individual turns of the coil (3) can be disposed and dimensioned so as to permit embossing of the circuit unit without restriction within an area (37, 38) conforming with the standard.

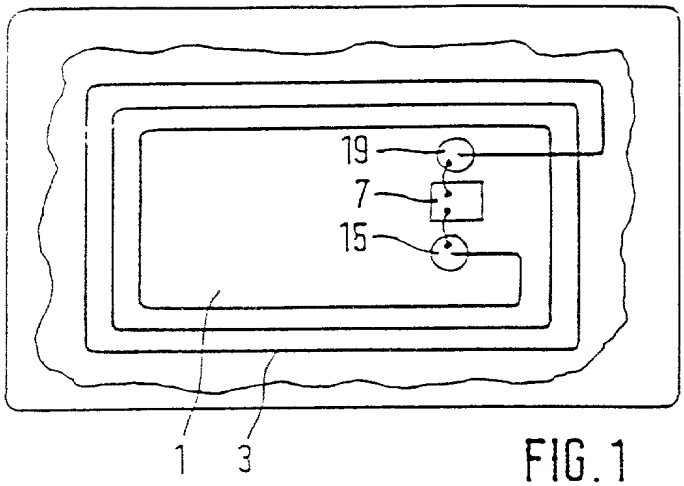

FIG. 1

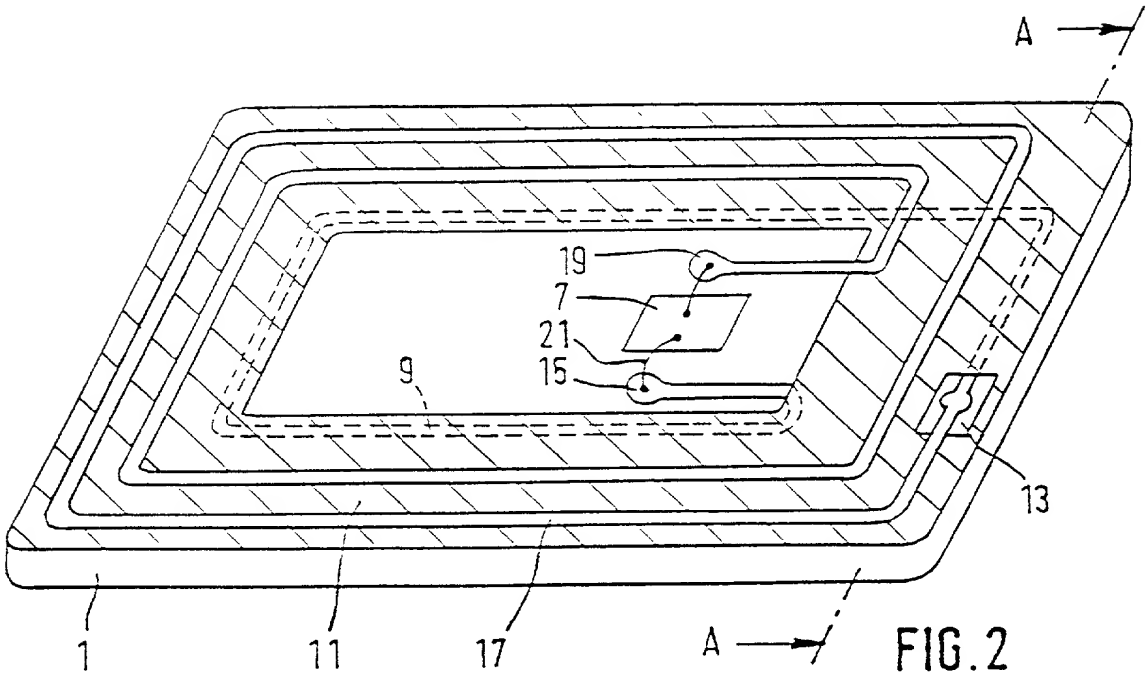

FIG. 2

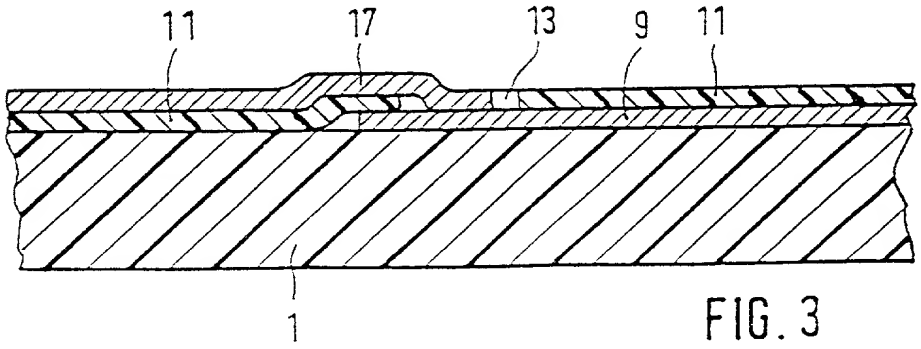

FIG. 3

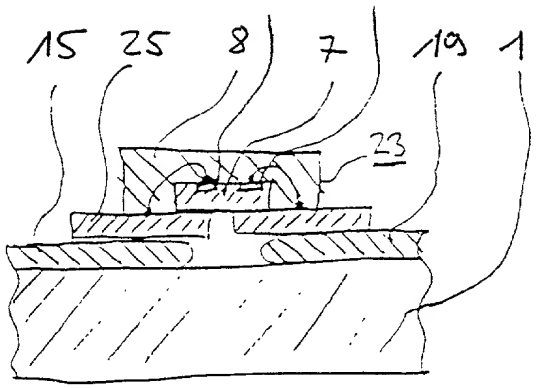

Fig. 4a

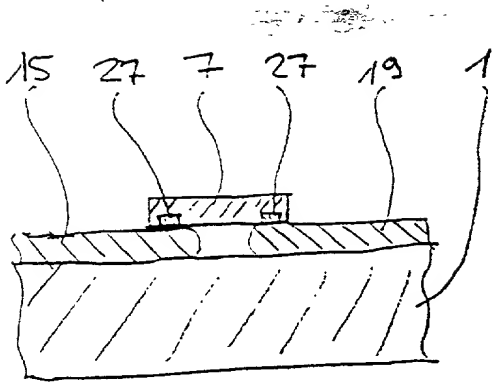

Fig. 4b

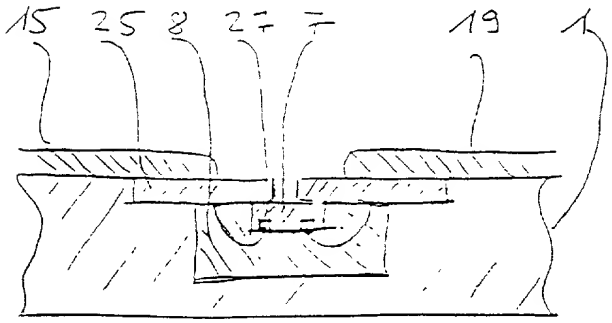

Fig 5a

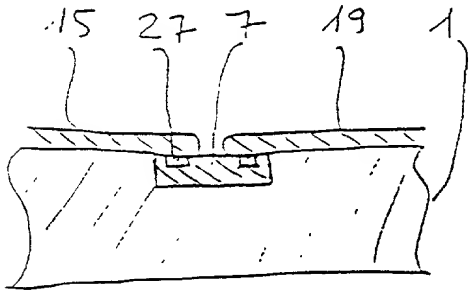

Fig 5b

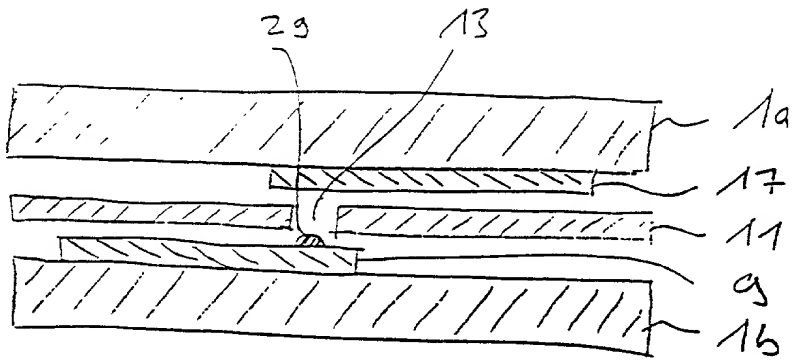

Fig 6

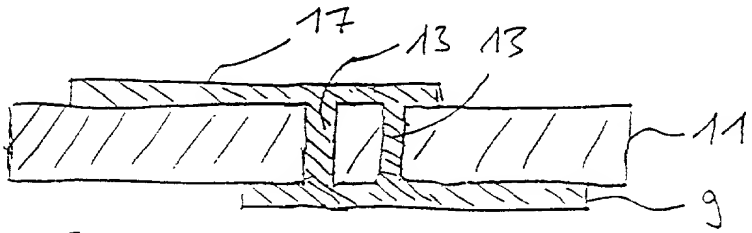

Fig. 7

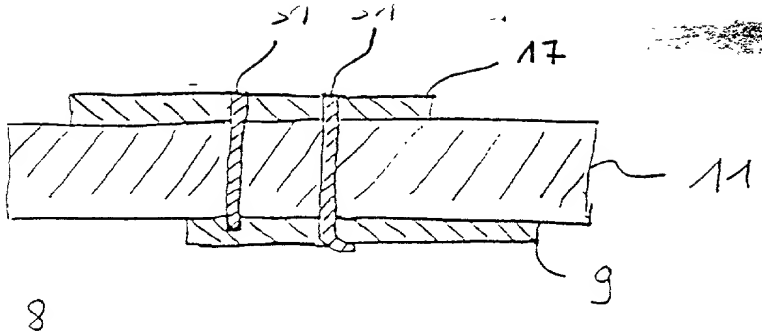

Fig. 8

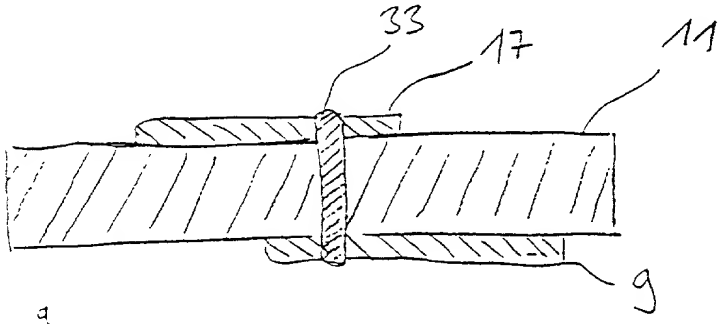

Fig. 9

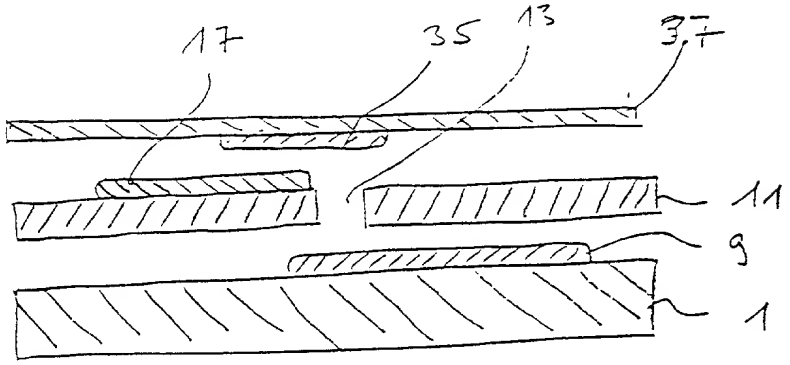

Fig. 10a

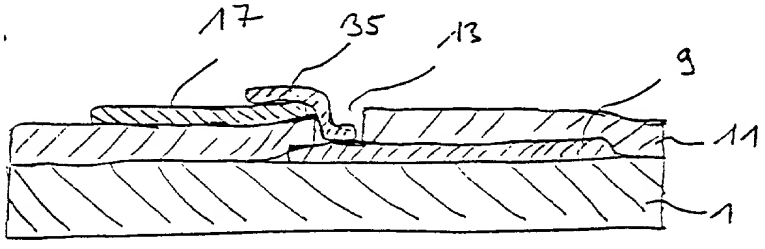

Fig 10b

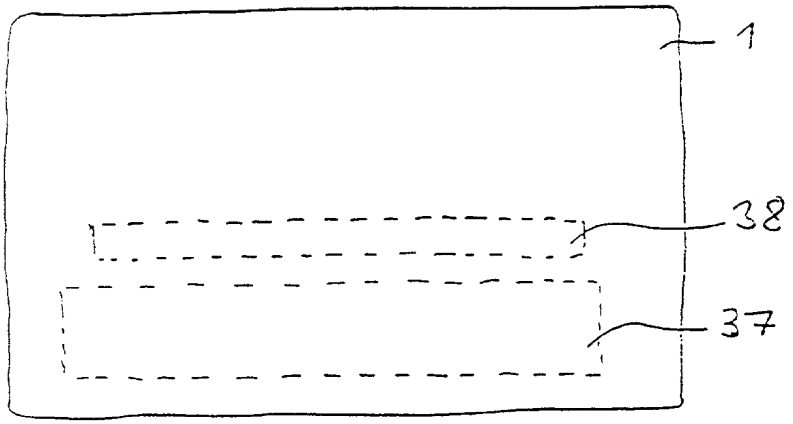

Fig. 11

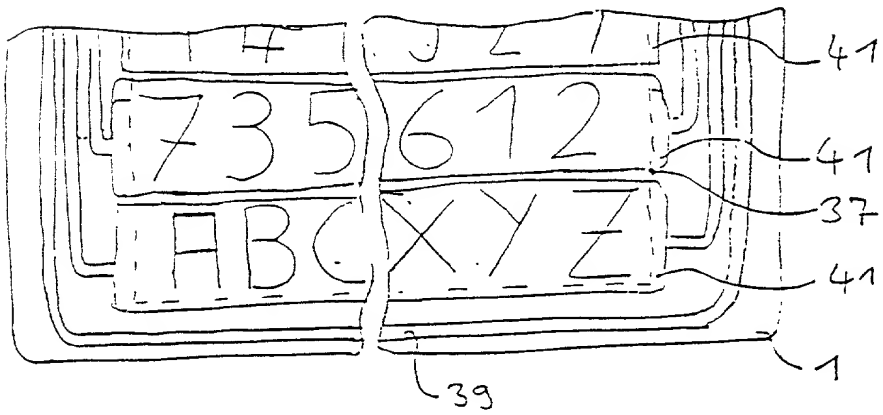

Fig. 12

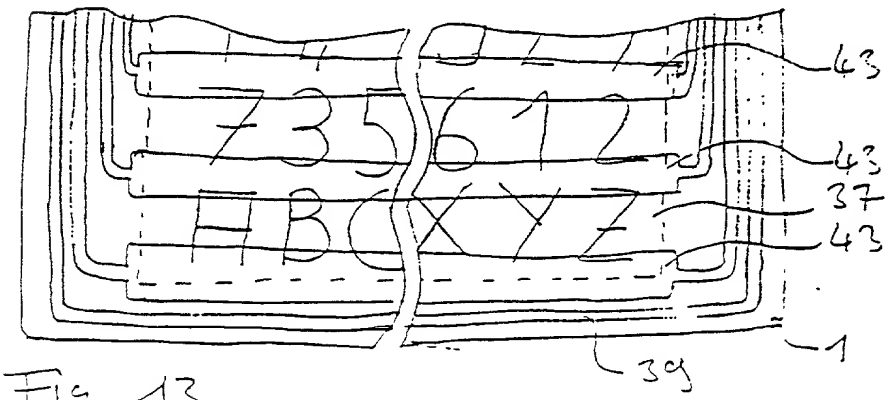

Fig. 13

Divisional Application of
Yahya HAGHIRI-TEHRANI et al.

APPENDIX OF CLAIMS

12(Amended Once). A method for producing a circuit unit comprising an insulating carrier substrate (1) on which a conductive coil (3) is located, and an integrated circuit (7) whose connection points (27) are electrically connected with the coil ends (15, 19) directly or via contacts (2S), [characterized by] comprising the following [method] steps:

a) applying a coil [layer] section (9) with at least one turn to the substrate (1),

b) covering at least the area of the applied coil [layer] section with an insulating layer (11) containing at least one opening (13) through which at least one of the covered turns of the coil [layer] section (9) is accessible,

c) applying to the insulating layer (11) a further coil [layer] section (17) with at least one turn which is electrically connected with the previously covered coil [layer] section (9) through the at least one opening (13),

[d) optionally repeating method steps b) and c) once or several times,]

e) electrically connecting the connection points (27) of the integrated circuit (7), or the contacts (25) of a module (23) containing the integrated circuit (7), with one end (15) of the coil [layer] section (9) located directly on the insulating substrate (1), on the one hand, and with one end (19) of the last applied coil [layer] section (17), on the other hand.

13(Amended Once). The method of claim 12, [characterized in that] wherein the electric connection between the coil [layers] sections (9, 17) [takes place] is carried out through the at least one opening (13) in the insulating layer (11) by laminating the insulating layer (11) or insulating layers (11) and the insulating substrate (1).

14(Amended Once). The method of claim 13, including disposing the [characterized in that] conductive material (29) [is additionally disposed] in the area of the at least one opening (13) before lamination.

15(Amended Once). The method of claim 12, including producing [characterized in that] the at least one opening (13) in the insulating layer (11) [is produced] before application of at least one of the coil [layers] sections (9, 17) separated by the insulating [layer] section (11), and filling the at least one opening (13) [is filled] with the coil material during application of at least one of the coil layers (9, 17).

16(Amended Once). The method of claim 12, including filling [characterized in that] the at least one opening (13) [is filled] with conductive material (33) after application of the coil [layers] sections (9, 17) so as to form an electric connection between the coil [layers] sections (9, 17).

17(Amended Once). The method of claim 12, including transferring [characterized in that] a conductive element (35) [is transferred] to the coil [layers] sections (9, 17) in such a way that the conductive element (35) forms an electric connection between the coil [layers] sections (9, 17) through the at least one opening (13).

18(Amended Once). The method of claim 12, including producing [characterized in that] the at least one opening (13) [is produced] by means of at least one wire (31) piercing the insulating layer (11) and at least partly the coil [layers] sections (9, 17) separated by the insulating layer (11), the wire (31) remaining in the insulating layer (11) and at least partly in the coil [layers] sections (9, 17) so as to form an electric connection between the coil [layers] sections (9, 17).

19(Amended Once). A method for producing a circuit unit comprising an insulating substrate (1) on which a conductive, flat coil (3) is located, and an integrated circuit (7) whose connection points (27) are electrically connected with the coil ends (15,19) directly or via contacts (25), [characterized by] comprising the steps of:

applying the coil (3) to the substrate (1) in such a way that the distance between the coil ends (15, 19) can be bridged by the connection points (27) of the integrated

circuit (7) or by the contacts (25) of a module (23) containing the integrated circuit (7), and

mounting the integrated circuit (7) or the module (23) on the coil ends (15, 19) in such a way that the connection points (27) of the integrated circuit (7) and the coil ends (15, 19) or the contacts (25) of the module (23) and the coil ends (15, 19) touch, and

forming an electric contact between the connection points (27) and the coil ends (15, 19) or the contacts (25) and the coil ends (15, 19) solely through this touching.

20(Amended Once). The method of claim 19, <u>including printing</u> [characterized in that] the coil (3) [is printed] on the substrate (1), and <u>mounting</u> the integrated circuit (7) or the module (23) [is mounted] before the [printing material] <u>printed coil</u> completely dries.

21(Amended Once). A method for producing a circuit unit comprising an insulating carrier substrate (1) on which a conductive, flat coil (3) is located, and an integrated circuit (7) whose connection points (27) are electrically connected with the coil ends (15, 19) directly or via contacts (25), [characterized by] <u>comprising</u> the steps of:

incorporating the integrated circuit (7) or a module (23) containing the integrated circuit (7) in the substrate (1) in such a way that the connection points (27) of the integrated circuit (3) or the contacts (25) of the module are flush with the surface of the substrate (1),

then applying the coil (3) to the substrate (1) in such a way that the coil ends (15, 19) at least partly cover the connection points (27) or the contacts (25), and

forming an electric contact between the connection points (27) and the coil ends (15, 19) or the contacts (25) and the coil ends (15, 19) solely through this direct touching.

22(Amended Once). The method of claim 21, [characterized in that the coil (3)

is printed on] wherein the step of applying the coil to the substrate is carried out by printing the coil on the substrate.

DECLARATION FOR PATENT APPLICATION AND APPOINTMENT OF ATTORNEY

As a below named inventor, I hereby declare that my residence, post office address and citizenship are as stated below next to my name; I believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention (Design, if applicable) entitled:

"A circuit unit and a method for producing a circuit unit"

the specification of which (check one):

☐ is attached hereto, or ☐ was filed on: as U.S. Application Number or PCT International Application Number:
and (if applicable) was amended on:

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment(s) referred to above. I acknowledge the duty to disclose information which is material to patentability as defined in *Title 37, Code of Federal Regulations, §1.56*. I hereby claim foreign priority benefits under *Title 35, United States Code §119* of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed.

PRIOR FOREIGN APPLICATION(S)			*PRIORITY CLAIMED*	
Number	*Country*	*Day/Month/Year Filed*	*Yes*	*No*
195 27 359.1	Germany	26/07/1995	x	

☐ Additional Priority Application(s) Listed on Following Page(s)

I HEREBY CLAIM THE BENEFIT UNDER TITLE 35 U.S. CODE §119(E) OF ANY U.S. PROVISIONAL APPLICATIONS LISTED BELOW.	
Application Number	*Day/Month/Year Filed*

☐ Additional Provisional Application(s) Listed on Following Page(s)

I hereby claim the benefit under *Title 35, United States Code, §120* of any United States application(s) or PCT international application(s) designating The United States of America listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in that/those prior application(s) in the manner provided by the first paragraph of *Title 35, United States Code, §112*, I acknowledge the duty to disclose information which is material to patentability as defined in *Title 37, Code of Federal Regulations, §1.56* which became available between the filing date of the prior application(s) and the national or PCT international filing date of this application:

Application Number	*Filing Date*	*Status - Patented, Pending or Abandoned*

☐ Additional US/PCT Priority Application(s) listed on Following Page(s)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under *section 1001 of title 18 of the United States Code* and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

POWER OF ATTORNEY: I (We) hereby appoint as my (our) attorneys, with full powers of substitution and revocation, to prosecute this application and transact all business in the Patent and Trademark Office connected therewith: J. Ernest Kenney, Reg. No. 19,179; Eugene Mar, Reg. No. 25,893; Richard E. Fichter, Reg. No. 26,382; Charles R. Wolfe, Jr., Reg. No. 28,680; Thomas J. Moore, Reg. No. 28,974; David E. Dougherty, Reg. No. 19,576; Bruce H. Troxell, Reg. No. 26,592; and

I(we) authorize my(our) attorneys to accept and follow instructions from _____ regarding any matter related to the preparation, examination, grant and maintenance of this application, any continuation, continuation-in-part or divisional based thereon, and any patent resulting therefrom, until I(we) or my(our) assigns withdraw this authorization in writing.

Send correspondence to: **BACON & THOMAS**
625 Slaters Lane - 4th Floor
Alexandria, VA 22314

Telephone Calls to:
(703) 683-0500

Full Name of First or Sole Inventor	*Citizenship*
Yahya HAGHIRI-TEHRANI	Iranian
Residence Address	*Post Office Address* ☒ *Same as Residence*
Winzererstr. 98 D-80797 Munich	
DATE July 25. 1996	*SIGNATURE* Yahya Haghiri-Tehrani

☐ *See following page(s) for additional joint inventors.*

CONTINUATION OF DECLARATION FOR PATENT APPLICATION AND APPOINTMENT OF ATTORNEY

PRIOR FOREIGN APPLICATION(S) (35 USC §119)			PRIORITY CLAIMED	
Number	Country	Day/Month/Year Filed	Yes	No

PRIOR PROVISIONAL APPLICATIONS 35 U.S. CODE §119(E)	
Application Number	Day/Month/Year Filed

PRIOR U.S. OR PCT INTERNATIONAL APPLICATIONS (35 U.S. CODE §120)		
Application Number	Filing Date	Status - Patented, Pending or Abandoned

Full Name of Joint Inventor Dr. Ando WELLING	Citizenship German
Residence Address Karl-Theodor-Str. 77 D-80803 Munich	Post Office Address ☒ Same as Residence
DATE 7/29/1996	SIGNATURE Ando Welling

Full Name of Joint Inventor	Citizenship
Residence Address	Post Office Address ☐ Same as Residence
DATE	SIGNATURE

Full Name of Joint Inventor	Citizenship
Residence Address	Post Office Address ☐ Same as Residence
DATE	SIGNATURE

Full Name of Joint Inventor	Citizenship
Residence Address	Post Office Address ☐ Same as Residence
DATE	SIGNATURE

☐ *See following pages for additional joint inventors/priority applications.*

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Yahya HAGHIRI-TEHRANI et al.

Serial No. 08/686,026

Filed: July 25, 1996

For: A CIRCUIT UNIT AND A METHOD FOR PRODUCING A CIRCUIT UNIT

WITHDRAWAL OF ATTORNEY

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

The undersigned, David E. Dougherty, Registration No. 19,576, hereby withdraws from representation of applicant(s) in the above-identified matter. The remaining attorneys designated in the Power of Attorney shall remain appointed to represent applicant(s) in this matter.

The undersigned, Mr. J. Ernest Kenney, represents that he is authorized to execute this paper on behalf of the remaining attorneys J. Ernest Kenney, Reg. No. 19,179; Eugene Mar, Reg. No. 25,893; Richard E. Fichter, Reg. No. 26,382; Charles R. Wolfe, Jr., Reg. No. 28,680; Thomas J. Moore, Reg. No. 28,974; Bruce H. Troxell, Reg. No. 26,592 and _____.

Please continue to send correspondence to BACON & THOMAS, 625 Slaters Lane, 4th Floor, Alexandria, Virginia 22314.

Respectfully submitted,

Date: June 4, 1996

David E. Dougherty
Registration No. 19,576
(703) 998-3302

Date: June 4, 1996

J. ERNEST KENNEY
Registration No. 19,179
(703) 683-0500

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